# AN1172

# DGD0280 Application Note

The DGD0280 is a high-speed, low-side, single gate driver with integrated LDO, capable of source current of 2.5A and sink current of 2.8A. Low-side gate drivers will optimally charge the gate of MOSFETs or IGBTs in a ground-based configuration. Below, (Figure 1) is an example application using the DGD0280 with a MOSFET in a power tool application; the aim of the DGD0280 is to optimally drive Q1 by quickly providing a charge on the gate when OUT becomes high. Typical PWM from the MCU control is 3.3V (with MCU supply provided by the DGD0280) and the DGD0280 converts the 3.3V PWM to the amplitude of Bat. Because of its high-speed performance, the DGD0280 is also well suited for low-voltage power supplies. In this application note, the important parameters needed to design in the DGD0280 are discussed. These include: gate driver component selection, decoupling capacitor discussion, and PCB layout suggestions.

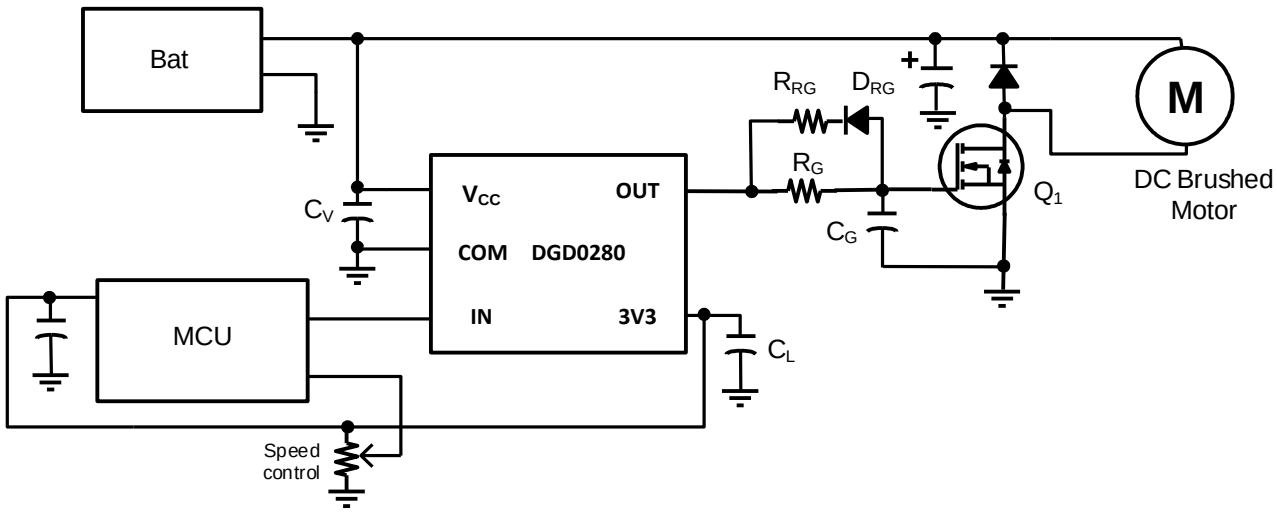


Figure 1. DGD0280 in DC brushed motor power tool application

## Gate Component Selection

The most crucial time in the gate drive is the turn on and turn off of the MOSFET or IGBT; the aim is to perform this function quickly, but with minimal noise and ringing when the MOSFET turns on. Too fast a rise/fall time can cause unnecessary ringing and poor EMI, and too slow a rise/fall time will increase switching losses in the MOSFET.

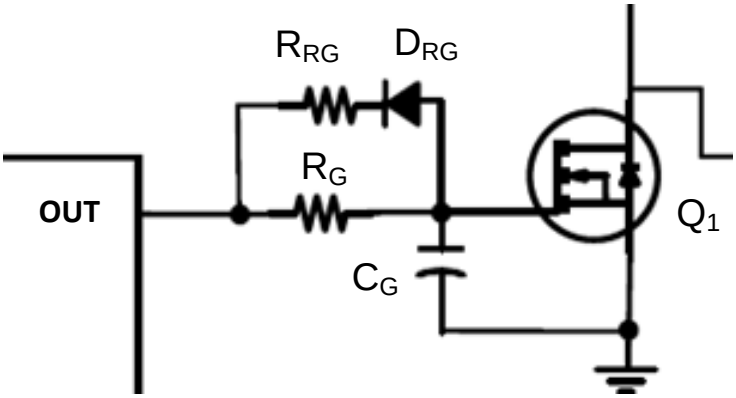


Figure 2. Gate drive components for DGD0280

Considering the gate driver components for the DGD0280 in Figure 2, with the careful selection of $R_G$ and $R_{RG}$, it is possible to selectively control the rise time and fall time of the gate drive to the MOSFET. For turn on, all current will go from the IC through $R_G$ and charge the MOSFET gate capacitance, hence increasing or decreasing $R_G$ will increase or decrease rise time in the application. With the addition of $D_{RG}$, the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitance, through $R_{RG}$ and $D_{RG}$ to the driver in the IC to GND. So, increasing or decreasing $R_{RG}$ will increase or decrease the fall time. Sometimes finer control is not needed and only $R_G$ needs to be used.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy or excessively ringing environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, contrasted with a slower rise time with better EMI, better noise performance but poorer efficiency. The exact value depends on the parameters of the application and system requirements. $R_G$ values are typically between 5Ω and 100Ω, optimal value decided by MOSFET gate capacitance and drive current of gate driver. $R_{RG}$ values are typically between 3Ω and 50Ω, optimal value decided by MOSFET gate capacitance and drive current of gate driver.

The gate to source capacitor $C_G$ is also used to minimize ringing and noise and to provide overall stability if the gate driver and MOSFET are not the optimal match. Most systems will not need $C_G$ (increasing the gate resistor can decrease ringing and provide system stability) but if required, then $C_G$ = 1nF is a good typical value.

## $V_{CC}$ Decoupling Capacitor

For optimal operation, $V_{CC}$ decoupling is crucial for all gate driver ICs. With poor decoupling, larger $V_{CC}$ transients will occur at the IC when switching.

As shown in Figure 1, $C_V$ is the decoupling capacitor. $C_V$ is used to decouple faster edge changes to $V_{CC}$ and should be a low ESR ceramic capacitor placed close to the $V_{CC}$ pin (see Layout section). This component provides stability when $V_{CC}$ is quickly pulled down with load from the IC; typical values are 0.1µF to 1µF.

## Internal LDO

To decrease the BOM and simplify the system design, the DGD0280 has an internal LDO to provide 3.3V (to 1% accuracy) to MCU and other associated circuits. Maximum suggested current draw is 15mA. During normal operation it is recommended to add a 0.1µF ceramic capacitor, close to the device between 3V3 and GND ($C_L$ in Figure 1).

## Inputs and outputs

There is only a single input (IN) for the DGD0280 and it is a very high impedance input with a pull-down resistor. The pull-down resistor on IN has an approximate value of 400kΩ (see Figure 3).

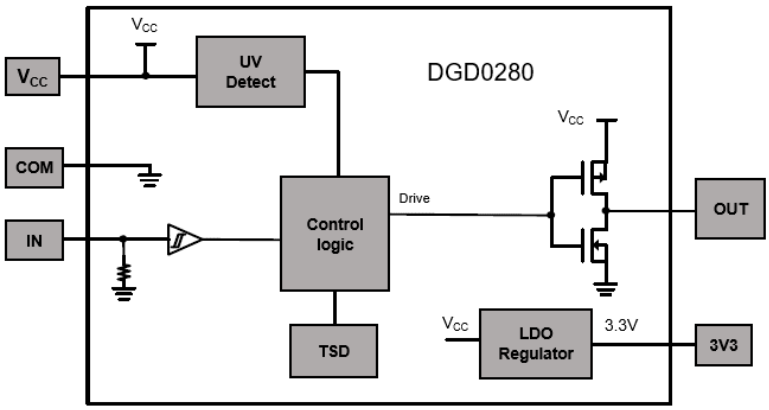


Figure 3. Input logic and functional block diagram for the DGD0280

## Matching Gate Driver with MOSFET or IGBT

### IC drive current and MOSFET/IGBT gate charge

Gate Driver ICs are defined by their output drive current, its ability to source current to the gate of the MOSFET/IGBT at turn on and to sink current from the gate of the MOSFET/IGBT at turn off. For the DGD0280 the source and sink drive current is $I_O$+ = 2.5A and IO- = 2.8A.

For a given MOSFET/IGBT, with the known drive current of the DGD0280, you can estimate how long it will take to turn on/off the MOSFET/IGBT with the equation:

$t = Q_g / I$

$Q_g$ = total charge of the MOSFET/IGBT as provided by the datasheet
I = sink/source capability of the gate driver IC
t = calculated rise/fall time with the given charge and drive current

For example, consider Diodes' DMN3009SK3, 30V, 20A, $Q_g$ = 42nC; and the DGD0280 $I_O$+ = 2.5A then $t_r$ = 17ns and for $I_O$- = 2.8A, $t_f$ = 15ns. These are estimates as the total charge given in the datasheet may not be the same conditions in the application. Also an addition of a gate resistor will increase the $t_r$ and $t_f$.

## PCB layout suggestions

Layout also plays a considerable role since unwanted noise coupling, unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. Figure 4 shows the DGD0280 with parasitic inductances in the high current path ($L_{P1}$, $L_{P2}$) which would be caused by inductance in the metal trace. Considering Figure 4, the length of the tracks in red should be minimized, and the decoupling capacitor ($C_V$) should be placed as close to the IC as possible as well as using low ESR ceramic capacitors. And finally, the gate resistor ($R_G$) should be a surface mount device. These suggestions will reduce the parasitics due to the PCB traces.

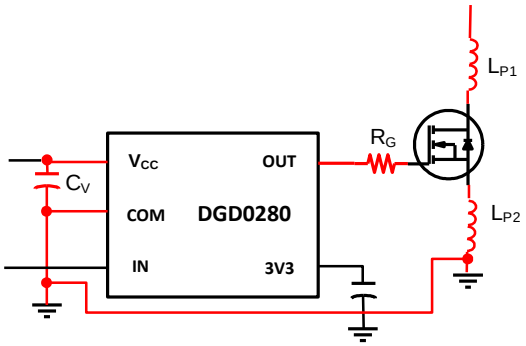


Figure 4. Layout suggestions for DGD0280, tracks in red should be as short as possible

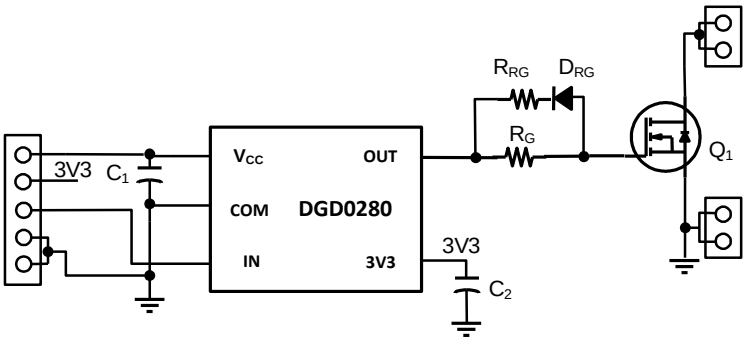


Figure 5. Schematic for layout example of DGD0280 shown in Figure 6.

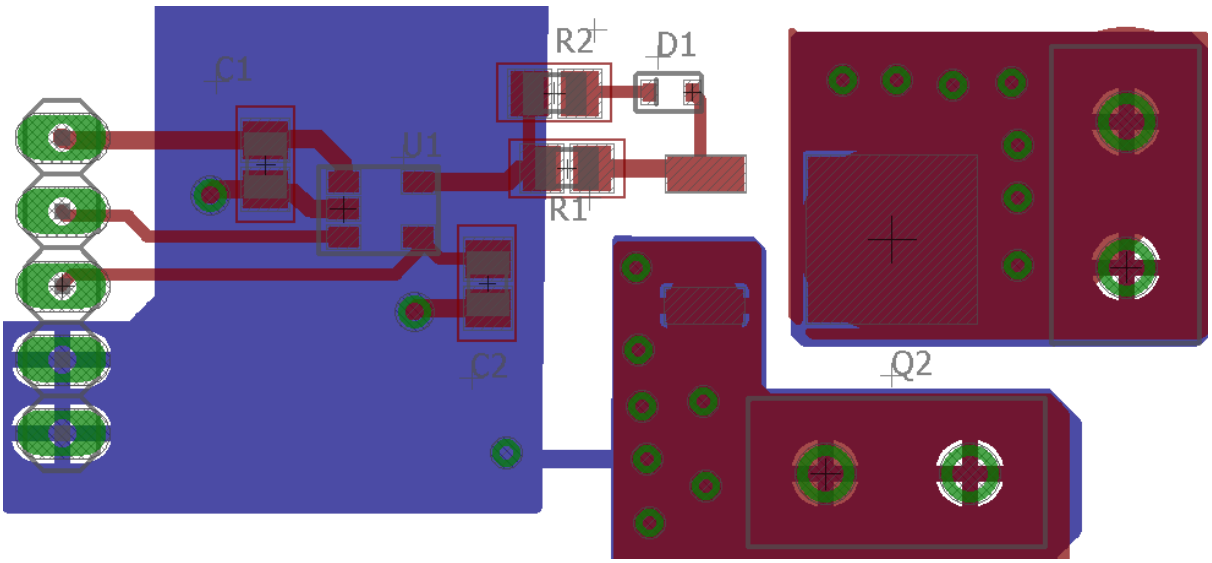


Figure 6. Layout for DGD0280 of the schematic shown in Figure 5.